National Semiconductor

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DAC0830/DAC0832
8-Bit µP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™).

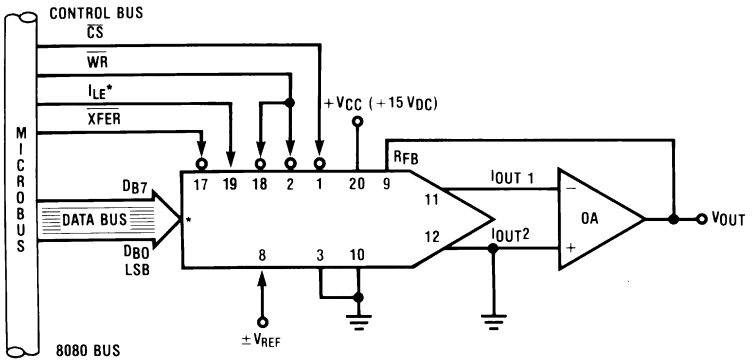
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates “STAND ALONE” (without µP) if desired
- Available in 20-pin small-outline or molded chip carrier package

Key Specifications

- Current settling time: 1 µs
- Resolution: 8 bits
- Linearity: 8, 9, or 10 bits (guaranteed over temp.)
- Gain Tempco: 0.0002% FS/˚C
- Low power dissipation: 20 mW
- Single power supply: 5 to 15 V_{DC}

Typical Application



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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65˚C to +150˚C
Package Dissipation at T_A=25˚C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability (Note 4)	800V
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260˚C
Dual-In-Line Package (ceramic)	300˚C
Surface Mount Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

Operating Conditions

Temperature Range	T_{MIN}≤T_A≤T_{MAX}
Part numbers with “LCN” suffix	0˚C to +70˚C
Part numbers with “LCWM” suffix	0˚C to +70˚C
Part numbers with “LCV” suffix	0˚C to +70˚C
Part numbers with “LCJ” suffix	−40˚C to +85˚C
Part numbers with “LJ” suffix	−55˚C to +125˚C
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF}=10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, T_{MIN}≤T_A≤T_{MAX}.** For all other limits T_A=25˚C.

Parameter	Conditions	See Note	V_{CC} = 4.75 V_{DC} V_{CC} = 15.75 V_{DC}		V_{CC} = 5 V_{DC} ±5% V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%	Limit Units
			Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER CHARACTERISTICS						
Resolution			8	8	**8**	bits
Linearity Error Max	Zero and full scale adjusted −10V≤V_{REF}≤+10V	4, 8				
DAC0830LJ & LCJ				**0.05**	**0.05**	% FSR
DAC0832LJ & LCJ				**0.2**	**0.2**	% FSR
DAC0830LCN, LCWM & LCV				0.05	**0.05**	% FSR
DAC0831LCN				0.1	**0.1**	% FSR
DAC0832LCN, LCWM & LCV				0.2	**0.2**	% FSR
Differential Nonlinearity Max	Zero and full scale adjusted −10V≤V_{REF}≤+10V	4, 8				
DAC0830LJ & LCJ				**0.1**	**0.1**	% FSR
DAC0832LJ & LCJ				**0.4**	**0.4**	% FSR
DAC0830LCN, LCWM & LCV				0.1	**0.1**	% FSR
DAC0831LCN				0.2	**0.2**	% FSR
DAC0832LCN, LCWM & LCV				0.4	**0.4**	% FSR
Monotonicity	−10V≤V_{REF} ≤+10V LJ & LCJ	4		**8**	**8**	bits
	−10V≤V_{REF} ≤+10V LCN, LCWM & LCV			8	**8**	bits
Gain Error Max	Using Internal R_{fb} −10V≤V_{REF}≤+10V	7	±0.2	±1	**±1**	% FS
Gain Error Tempco Max	Using internal R_{fb}		**0.0002**		**0.0006**	%

Electrical Characteristics (Continued)

V_{REF}=10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits T_A=25˚C.

Parameter		Conditions	See Note	V_{CC} = 4.75 V_{DC} V_{CC} = 15.75 V_{DC}		V_{CC} = 5 V_{DC} ±5% V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%	Limit Units
				Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER CHARACTERISTICS							
							FS/˚C
Power Supply Rejection		All digital inputs latched high					
		V_{CC}=14.5V to 15.5V		0.0002	0.0025		%
		11.5V to 12.5V		0.0006			FSR/V
		4.5V to 5.5V		0.013	0.015		
Reference	Max			**15**	**20**	**20**	kΩ
Input	Min			**15**	**10**	**10**	kΩ
Output Feedthrough Error		V_{REF}=20 Vp-p, f=100 kHz All data inputs latched low		3			mVp-p
Output Leakage Current Max	I_{OUT1}	All data inputs latched low	LJ & LCJ	10		**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
	I_{OUT2}	All data inputs latched high	LJ & LCJ			**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
Output Capacitance	I_{OUT1} I_{OUT2}	All data inputs latched low			45 115			pF
	I_{OUT1} I_{OUT2}	All data inputs latched high			130 30			pF
DIGITAL AND DC CHARACTERISTICS								
Digital Input Voltages	Max	Logic Low	LJ: 4.75V			**0.6**		V_{DC}
			LJ: 15.75V			**0.8**		
			LCJ: 4.75V			**0.7**		
			LCJ: 15.75V			**0.8**		
			LCN, LCWM, LCV			0.95	**0.8**	
	Min	Logic High	LJ & LCJ			**2.0**	**2.0**	V_{DC}
			LCN, LCWM, LCV			1.9	**2.0**	
Digital Input Currents	Max	Digital inputs <0.8V						
			LJ & LCJ		−50	**−200**	**−200**	µA
			LCN, LCWM, LCV			−160	**−200**	µA
		Digital inputs>2.0V						
			LJ & LCJ		0.1	**+10**	**+10**	µA
			LCN, LCWM, LCV			+8	**+10**	
Supply Current Drain	Max		LJ & LCJ		1.2	**3.5**	**3.5**	mA
			LCN, LCWM, LCV			1.7	**2.0**	

Electrical Characteristics

V_{REF}=10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits T_A=25˚C.

Symbol	Parameter	Conditions	See Note	V_{CC}=15.75 V_{DC}		V_{CC}=12 V_{DC}±5% to 15 V_{DC} ±5%	V_{CC}=4.75 V_{DC}		V_{CC}=5 V_{DC}±5%	Limit Units
				Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
AC CHARACTERISTICS										
t_s	Current Setting Time	V_{IL}=0V, V_{IH}=5V		1.0			1.0			µs
t_W	Write and XFER Pulse Width Min	V_{IL}=0V, V_{IH}=5V	11 9	100	250 **320**	**320**	375	600 **900**	**900**	ns
t_{DS}	Data Setup Time Min	V_{IL}=0V, V_{IH}=5V	9	100	250 **320**	**320**	375	600 **900**	**900**	ns
t_{DH}	Data Hold Time Min	V_{IL}=0V, V_{IH}=5V	9		30 **30**			50 **50**		ns
t_{CS}	Control Setup Time Min	V_{IL}=0V, V_{IH}=5V	9	110	250 **320**	**320**	600	900 **1100**	**1100**	ns
t_{CH}	Control Hold Time Min	V_{IL}=0V, V_{IH}=5V	9	0	0 **0**	**10**	0	0 **0**		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 125˚C (plastic) or 150˚C (ceramic), and the typical junction-to-ambient thermal resistance of the J package when board mounted is 80˚C/W. For the N package, this number increases to 100˚C/W and for the V package this number is 120˚C/W.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Guaranteed at V_{REF}=±10 V_{DC} and V_{REF}=±1 V_{DC}.

Note 8: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)". This guarantees that after performing a zero and full scale adjustment (see Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within 0.05%xV_{REF} of a straight line which passes through zero and full scale.

Note 9: **Boldface** tested limits apply to the LJ and LCJ suffix parts only.

Note 10: A 100nA leakage current with R_{fb}=20k and V_{REF}=10V corresponds to a zero error of $(100x10^{-9}x20x10^{3})x100/10$ which is 0.02% of FS.

Note 11: The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 12: Typicals are at 25˚C and represent most likely parametric norm.

Note 13: Human body model, 100 pF discharged through a 1.5 kΩ resistor.