2N3055A (NPN)
MJ15015, MJ15016 (PNP)

MJ15015 and MJ15016 are Preferred Devices

Complementary Silicon High-Power Transistors

These PowerBase™ complementary transistors are designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc−to−dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055.

Features

- Current−Gain − Bandwidth−Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) − NPN
  = 2.2 MHz (Min) − PNP
- Safe Operating Area − Rated to 60 V and 120 V, Respectively
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N3055A MJ15015, MJ15016	V_{CEO}	 60 120	Vdc
Collector−Base Voltage 2N3055A MJ15015, MJ15016	V_{CBO}	 100 200	Vdc
Collector−Emitter Voltage Base Reversed Biased 2N3055A MJ15015, MJ15016	V_{CEV}	 100 200	Vdc
Emitter−Base Voltage	V_{EBO}	7.0	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current	I_B	7.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C 2N3055A Total Device Dissipation @ T_C = 25°C Derate above 25°C MJ15015, MJ15016	P_D	115 0.65 180 1.03	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.52	0.98	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data. (2N3055A)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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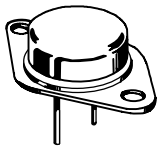
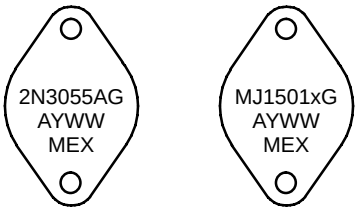
http://onsemi.com

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60, 120 VOLTS − 115, 180 WATTS



TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAMS



2N3055A = Device Code
MJ1501x = Device Code
x = 5 or 6
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (Note 2)					
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 200 mAdc, I_B = 0)	2N3055A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	− −	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	 2N3055A MJ15015, MJ15016	I_{CEO}	 − −	 0.7 0.1	mAdc
Collector Cutoff Current (Note 3) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A MJ15015, MJ15016	I_{CEV}	− −	5.0 1.0	mAdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N3055A MJ15015, MJ15016	I_{CEV}	 − −	 30 6.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A MJ15015, MJ15016	I_{EBO}	− −	5.0 0.2	mAdc
SECOND BREAKDOWN (Note 3)					
Second Breakdown Collector Current with Base Forward Biased (t = 0.5 s non−repetitive) (V_{CE} = 60 Vdc)	 2N3055A MJ15015, MJ15016	$I_{S/b}$	 1.95 3.0	 − −	Adc
ON CHARACTERISTICS (Note 2 and 3)					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 10 20 5.0	 70 70 −	−
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc) (I_C = 15 Adc, I_B = 7.0 Adc)		$V_{CE(sat)}$	 − − −	 1.1 3.0 5.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
DYNAMIC CHARACTERISTICS (Note 3)					
Current−Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
SWITCHING CHARACTERISTICS (2N3055A only) (Note 3)					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	−	0.5	μs
Rise Time		t_r	−	4.0	μs
Storage Time		t_s	−	3.0	μs
Fall Time		t_f	−	6.0	μs

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
3. Indicates JEDEC Registered Data. (2N3055A)

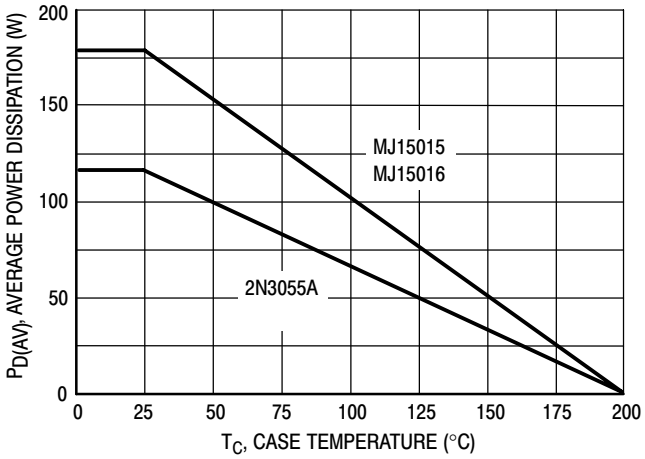


Figure 1. Power Derating

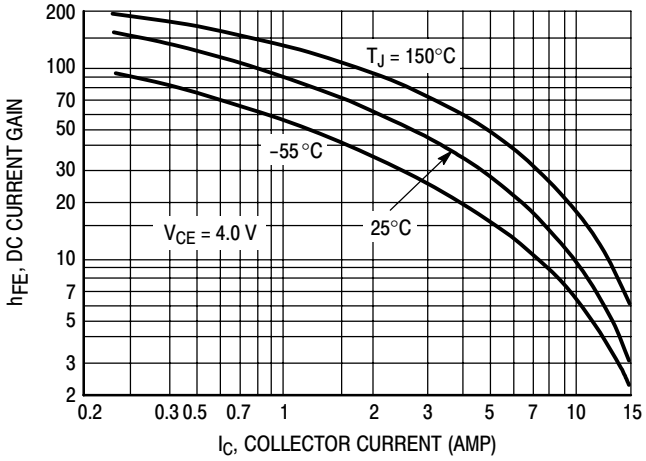


Figure 2. DC Current Gain

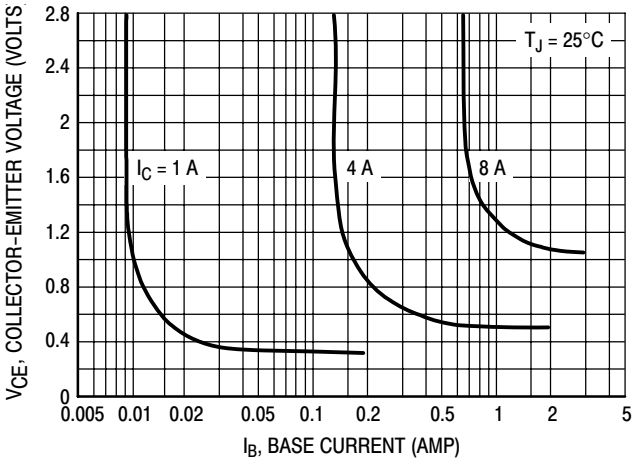


Figure 3. Collector Saturation Region

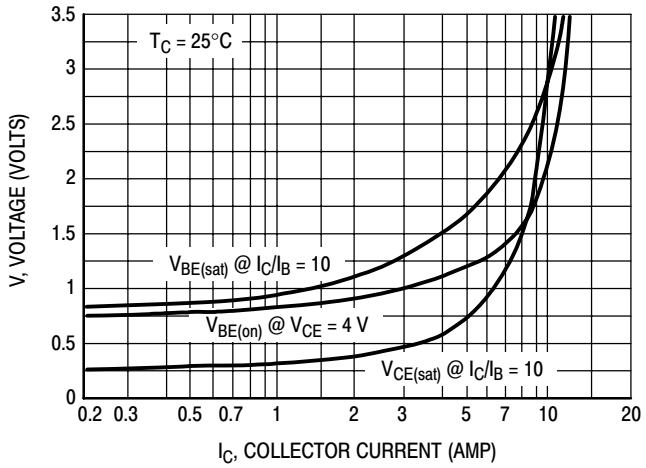


Figure 4. “On” Voltages

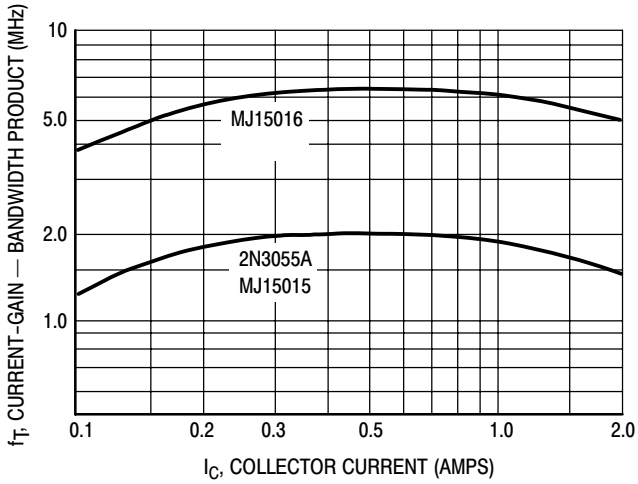


Figure 5. Current−Gain — Bandwidth Product

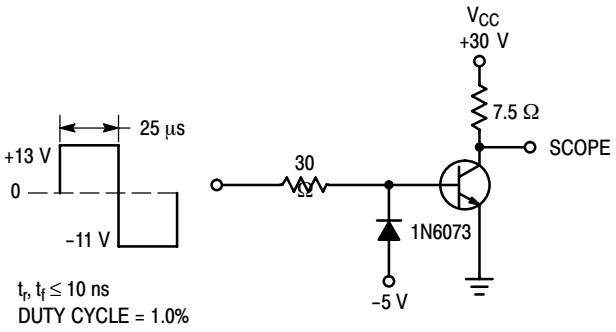


Figure 6. Switching Times Test Circuit (Circuit shown is for NPN)

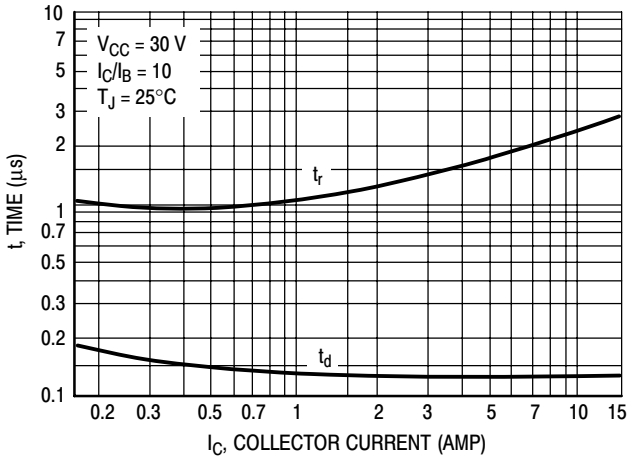


Figure 7. Turn−On Time

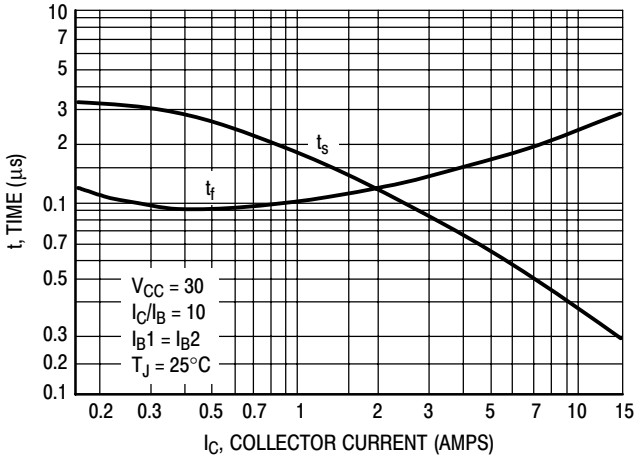


Figure 8. Turn−Off Times

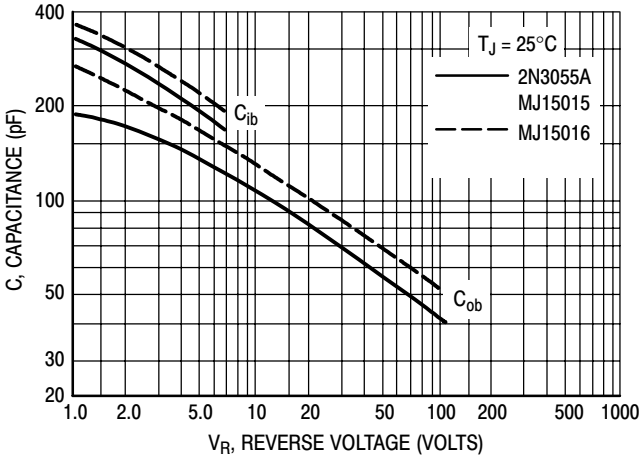


Figure 9. Capacitances

COLLECTOR CUT−OFF REGION

NPN

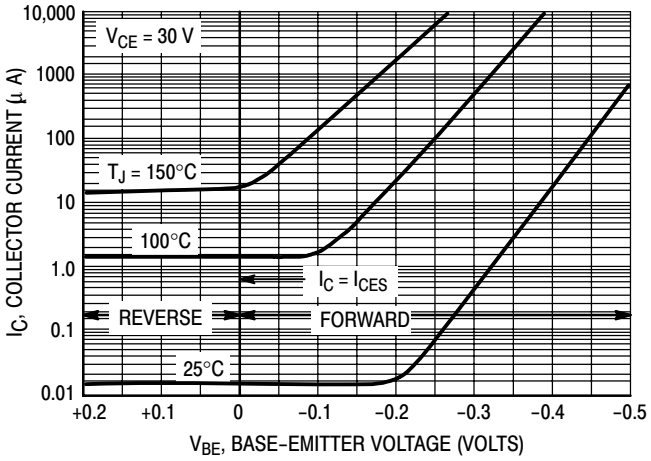


Figure 10. 2N3055A, MJ15015

PNP

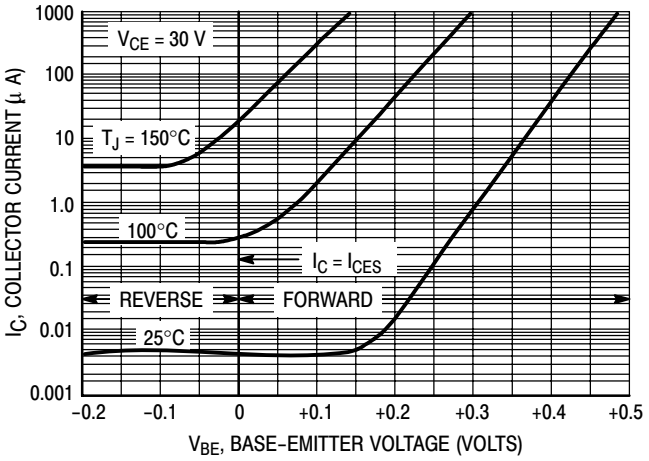


Figure 11. MJ15016

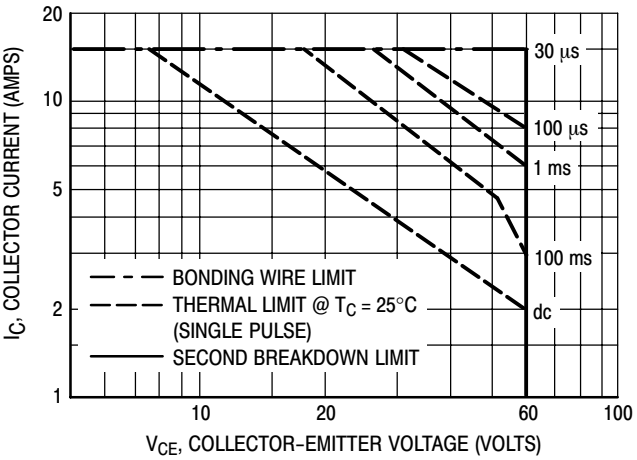


Figure 12. Forward Bias Safe Operating Area 2N3055A

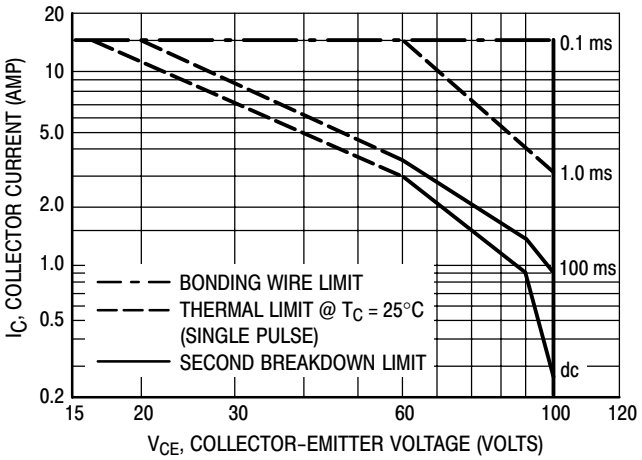


Figure 13. Forward Bias Safe Operating Area MJ15015, MJ15016

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

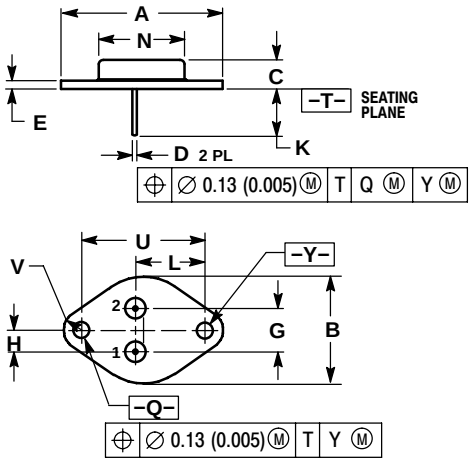
The data of Figures 12 and 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

ORDERING INFORMATION

Device	Package	Shipping
2N3055A	TO−204	100 Units / Tray
2N3055AG	TO−204 (Pb−Free)	
MJ15015	TO−204	100 Units / Tray
MJ15015G	TO−204 (Pb−Free)	
MJ15016	TO−204	
MJ15016G	TO−204 (Pb−Free)	

PACKAGE DIMENSIONS

TO−204 (TO−3)
CASE 1−07
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
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